REMARKS

Claims 11 to 41 have been canceled without prejudice in favor of new claims 52 to 63 and, in view of the withdrawal of the requirement for restriction, claims 1 to 10 have been reinserted as new claims 42 to 51 respectively with claim 42 being in amended form. No fee for claims is believed to be required since 5 independent claims were originally filed and paid for. However, should a fee be required, please charge same to Deposit Account No. 20-0668.

Claims 11 to 41 were rejected under 35 U.S.C. 102(e) as being anticipated by Voldman et al. (U.S. 6,198,136 B1). The rejection is respectfully traversed.

Claim 42 requires, among other features, an electrostatic discharge device disposed in the substrate at least partially disposed beneath the bond pad. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 42 further requires an I/O buffer formed in the substrate and connected to the bond pad providing communication between the bond pad and circuitry disposed in the substrate, the circuitry being positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claims 43 to 51 depend from claim 42 and therefore define patentably over Voldman et al. for the reasons presented above with reference to claim 42.

Claim 52 requires, among other features, an electrostatic discharge device and an I/O buffer disposed between the scribe region and the core region and laterally of the

bond pad relative to the core region and the scribe region. No such feature is taught or suggested by Voldman et al. either alone or in the total combination as claimed.

Claim 53 requires, among other features, an electrostatic discharge device disposed at least partially beneath the bond pad and an I/O buffer disposed between the scribe region and the core region. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 54 depends from claim 53 and therefore defines patentably over Voldman et al. for at least the reasons stated above with reference to claim 53.

In addition, claim 54 further limits claim 53 by requiring that the I/O buffer be further disposed laterally of the bond pad relative to the core region and the scribe region. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 55 requires, among other features, an electrostatic discharge device and an I/O buffer disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 56 requires, among other features, an electrostatic discharge device disposed at least partially beneath the bond pad and an I/O buffer disposed between the scribe region and the core region. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 57 depends from claim 56 and therefore defines patentably over Voldman et al. for at least the reasons presented above with reference to claim 56.

In addition, claim 57 further limits claim 56 by requiring that the I/O buffer be further disposed laterally of the bond pad relative to the core region and the scribe region. No such feature is taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 58 requires, among other steps, an electrostatic discharge device and an I/O buffer disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region. No such steps are taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 59 requires, among other features, an electrostatic discharge device disposed at least partially beneath the bond pad and an I/O buffer disposed between the scribe region and the core region. No such steps are taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 60 depends from claim 59 and therefore defines patentably over Voldman et al. for at least the reasons presented above with reference to claim 59.

In addition, claim 60 further limits claim 59 by requiring that the I/O buffer be further disposed laterally of the bond pad relative to the core region and the scribe region. No such steps are taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 61 requires, among other steps, providing an electrostatic discharge device and providing an I/O buffer disposed between the scribe region and the core region and laterally of the bond pad relative to the core region and the scribe region. No such steps are taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 62 requires, among other steps, providing an electrostatic discharge device disposed at least partially beneath the bond pad and providing an I/O buffer disposed between the scribe region and the core region. No such steps are taught or suggested by Voldman et al. either alone or in the combination as claimed.

Claim 63 depends from claim 62 and therefore defines patentably over Voldman et al. for at least the reasons presented above with reference to claim 62.

In addition, claim 63 further limits claim 62 by requiring that the I/O buffer be further disposed laterally of the bond pad relative to the core region and the scribe region. No such steps are taught or suggested by Voldman et al. either alone or in the combination as claimed.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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42. An integrated circuit having a plurality of I/O modules, comprising:

a substrate;

a bond pad disposed on said substrate;

an electrostatic discharge device disposed in the substrate, the electrostatic discharge device being at least partially disposed beneath the bond pad;

an I/O buffer formed in the substrate and connected to the bond pad, the I/O buffer providing communication between the bond pad and circuitry disposed in the substrate, wherein the circuitry is positioned substantially adjacent to both the electrostatic discharge device and the I/O buffer.

43. The integrated circuit of claim 42 wherein the substrate is a silicon substrate.

44, The integrated circuit of claim 42 wherein the I/O buffer is an output buffer.

45. The integrated circuit of claim 42 wherein the I/O buffer is an input buffer.

46. The integrated circuit of claim 42 wherein the I/O buffer is a complementary output buffer.

47. The integrated circuit of claim 42 wherein the circuitry is CMOS circuitry.

48. The integrated circuit of claim 42 wherein the circuitry is BiCMOS circuitry.

49. The integrated circuit of claim 42 wherein the circuitry is an application specific integrated circuit.

50. The integrated circuit of claim 42 wherein the circuitry is digital signal processor.

51. The integrated circuit of claim 42 wherein the entire surface of the substrate beneath the bond pad is occupied by the electrostatic discharge device.

52. A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

53. A semiconductor wafer which comprises:

a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; each of said integrated circuits including:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

54. The semiconductor wafer of claim 53 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

55 An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

56 An integrated circuit which comprises:

a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

57. The circuit of claim 56 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

58. A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device; and

an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

59. A method of fabricating a semiconductor wafer which comprises the steps of:

providing a plurality of integrated circuits, each of said integrated circuits separated from the other of said integrated circuits by a scribe region at the periphery of each said integrated circuit; and providing in each of said integrated circuits:

a centrally disposed core region;

at least one bond pad disposed between said core region and said scribe region;

an electrostatic discharge device disposed at least partially beneath said bond pad; and

an I/O buffer disposed between said scribe region and said core region.

60. The method of claim 59 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.

61 A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing an electrostatic discharge device; and

providing an I/O buffer disposed between said scribe region and said core region and laterally of said bond pad relative to said core region and said scribe region..

62 A method of fabricating an integrated circuit which comprises the steps of:

providing a semiconductor substrate which includes a scribe at the periphery of said substrate and a centrally disposed core region;

providing at least one bond pad disposed between said core region and said scribe region;

providing an electrostatic discharge device disposed at least partially beneath said bond pad; and

providing an I/O buffer disposed between said scribe region and said core region.

63. The method of claim 62 wherein said I/O buffer is further disposed laterally of said bond pad relative to said core region and said scribe region.